174/153 Cont.2

Corrected

FAST SIGNAL CONDUCTOR NETWORKS FOR PROGRAMMABLE LOGIC DEVICES

This application is a continuation of United States patent application No. 09/765,796, filed February 28, 2001, which is now a U.S. Patent 6,373,280 which is hereby incorporated by reference herein in its entirety, and which is a continuation of United States patent application No. 09/287,048, filed April 6, 1999, which is now a U.S. patent 6,225,822 which claims the benefit of United States provisional patent application No. 60/109,417, filed November 18, 1998.

Background of the Invention

This invention relates to programmable logic integrated circuit devices, and more particularly to the organization of particular types of interconnection conductors on such devices.

Programmable logic devices with areas of programmable logic disposed on the device in a two-dimensional array of intersecting rows and columns of such areas are well known as shown, for example, by Cliff et al. U.S. patent 5,689,195, which is hereby incorporated by reference herein in its entirety. Advances in integrated circuit fabrication technology are making it possible to make such programmable logic devices both larger and denser. For example, more and more areas of programmable logic can be put on such